

### FEATURES

- Eight 13-Bit DACs in One Package
- Full 13-Bit Performance without Adjustments
- Buffered Voltage Outputs
- Offset Adjust for Each DAC Pair
- $\pm 5$  V Supply Operation
- Unipolar or Bipolar Output Swing to  $\pm 4.5$  V
- Output Settling to 1/2 LSB in  $5 \mu\text{s}$
- Double Buffered Digital Inputs
- Microprocessor and TTL/CMOS Compatible
- Asynchronous Load Facility using  $\overline{\text{LDAC}}$  Inputs
- Clear Function to User-Defined Voltage
- Power-On-Reset, Outputs Power Up at DUTGND
- 44-Lead PLCC Package
- Pin Compatible with MAX547

### APPLICATIONS

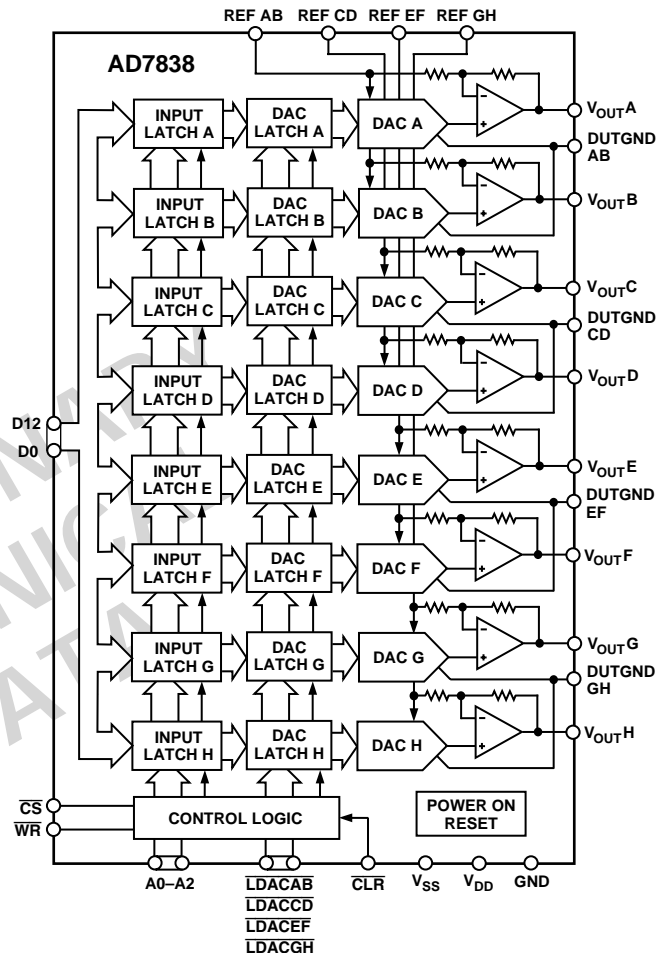
- Process Control
- Automatic Test Equipment
- General Purpose Instrumentation
- Digital Offset and Gain Adjustment
- Arbitrary Function Generators
- Avionics Equipment

### GENERAL DESCRIPTION

The AD7838 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). The output voltages are provided through on-chip precision output amplifiers into which an external offset voltage can be inserted via the DUTGND pins. The AD7838 operates from a  $\pm 5 \text{ V} \pm 5\%$  supply. Bipolar output voltages with up to  $\pm 4.5 \text{ V}$  voltage swing can be achieved with no external components. The AD7838 has four separate reference inputs; each is connected to two DACs, providing different scale output voltages for every DAC pair.

The AD7838 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous  $\overline{\text{LDAC}}$  input transfers data from the input latch to the DAC latch. The four  $\overline{\text{LDAC}}$  inputs each control two DACs, and all DAC latches can be updated simultaneously by asserting

### FUNCTIONAL BLOCK DIAGRAM



all  $\overline{\text{LDAC}}$  pins. An asynchronous clear input resets the output of all eight DACs to the relevant DUTGND. Asserting  $\overline{\text{CLR}}$  resets both the DAC and the input latch to bipolar zero (1000 Hex). On power-up, reset circuitry performs the same function as  $\overline{\text{CLR}}$ . All logic inputs are TTL/CMOS compatible.

The AD7838 is available in a 44-lead PLCC package.

REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

# AD7838—SPECIFICATIONS

( $V_{DD} = +5\text{ V}$ ;  $V_{SS} = -5\text{ V}$ ;  $DUTGNDXX = GND = 0\text{ V}$ ;  $R_L = 10\text{ k}\Omega$  and  $C_L = 50\text{ pF}$  to GND,  $T_A^1 = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .)

Parameter	B	Units	Test Conditions/Comments
<b>ACCURACY</b>			
Resolution	13	Bits	
Relative Accuracy	$\pm 2$	LSB max	Typically $\pm 0.5$ LSB
Differential Nonlinearity	$\pm 1$	LSB max	Guaranteed Monotonic Over Temperature
Bipolar Zero-Code Error	$\pm 20$	LSB max	Typically $\pm 5$ LSB
Gain Error	$\pm 8$	LSB max	Typically $\pm 1$ LSB
$V_{DD}$ Power Supply Rejection <sup>2</sup>	$\pm 0.0025$	%/% max	$\Delta\text{Gain}/\Delta V_{DD}$
$V_{SS}$ Power Supply Rejection <sup>2</sup>	$\pm 0.0025$	%/% max	$\Delta\text{Gain}/\Delta V_{SS}$
Load Regulation	0.3	LSB typ	$R_L = \text{Unloaded to } 10\text{ k}\Omega$
<b>REFERENCE INPUTS<sup>3, 4</sup></b>			
Input Range	DUTGND	V min	
	$V_{DD}$	V max	
Input Impedance	5	k $\Omega$ min	
<b>OUTPUT CHARACTERISTICS</b>			
Maximum Output Voltage	$V_{DD} - 0.5$	V max	
Minimum Output Voltage	$V_{SS} + 0.5$	V min	
<b>DYNAMIC PERFORMANCE</b>			
Voltage Output Slew Rate	3	V/ $\mu\text{s}$ typ	
Output Settling Time	5	$\mu\text{s}$ typ	Settling to 0.5 LSB of Full Scale <sup>5</sup>
Digital Feedthrough	5	nV-s typ	
Digital Crosstalk	5	nV-s typ	
<b>DIGITAL INPUTS</b>			
$V_{INH}$ , Input High Voltage	2.4	V min	
$V_{INL}$ , Input Low Voltage	0.8	V max	
$I_{INH}$ , Input Current	$\pm 1$	$\mu\text{A}$ max	$V_{IN} = 0\text{ V}$ or $V_{DD}$
$C_{IN}$ , Input Capacitance <sup>6</sup>	10	pF max	
<b>POWER REQUIREMENTS</b>			
$V_{DD}$	5	V nom	$\pm 5\%$ for Specified Performance
$V_{SS}$	-5	V nom	$\pm 5\%$ for Specified Performance
$I_{DD}$	44	mA max	Typically 14 mA
$I_{SS}$	40	mA max	Typically 11 mA

## NOTES

<sup>1</sup>Temperature Range for B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>PSRR is tested by changing the respective supply voltage by  $\pm 5\%$ .

<sup>3</sup>For best performance, REFxx should be greater than DUTGNDxx by 2 V and less than  $V_{DD} - 0.6\text{ V}$ . The device operates with reference inputs outside this range, but performance may degrade.

<sup>4</sup>Reference input resistance is code dependent.

<sup>5</sup>Typical settling time with 1000 pF capacitive load is 10  $\mu\text{s}$ .

<sup>6</sup>Guaranteed by design, not production tested.

Specifications subject to change without notice.

## TIMING SPECIFICATIONS<sup>1</sup> ( $V_{DD} = +5\text{ V}$ ; $V_{SS} = -5\text{ V}$ ; $DUTGND = GND = 0\text{ V}$ , $REF_{XX} = 4.096\text{ V}$ )

Parameter	Limit at $T_{MIN}$ , $T_{MAX}$	Units	Description
$t_1$	10	ns min	Address Valid to $\overline{WR}$ Setup Time
$t_2$	0	ns min	Address Valid to $\overline{WR}$ Hold Time
$t_3$	50	ns min	$\overline{CS}$ Pulse Width
$t_4$	50	ns min	$\overline{WR}$ Pulse Width
$t_5$	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
$t_6$	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
$t_7$	50	ns min	Data Valid to $\overline{WR}$ Setup Time
$t_8$	0	ns min	Data Valid to $\overline{WR}$ Hold Time
$t_9$	5	$\mu\text{s typ}$	Output Settling Time
$t_{10}$	100	ns min	$\overline{CLR}$ Pulse Width
$t_{11}$	50	ns min	$\overline{LDAC}$ Pulse Width

### NOTES

<sup>1</sup>All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of 5 V) and timed from a voltage level of 1.6 V. Timing applies for all grades of the part.

<sup>2</sup>Rise and fall times should be no longer than 50 ns.

Specifications subject to change without notice.

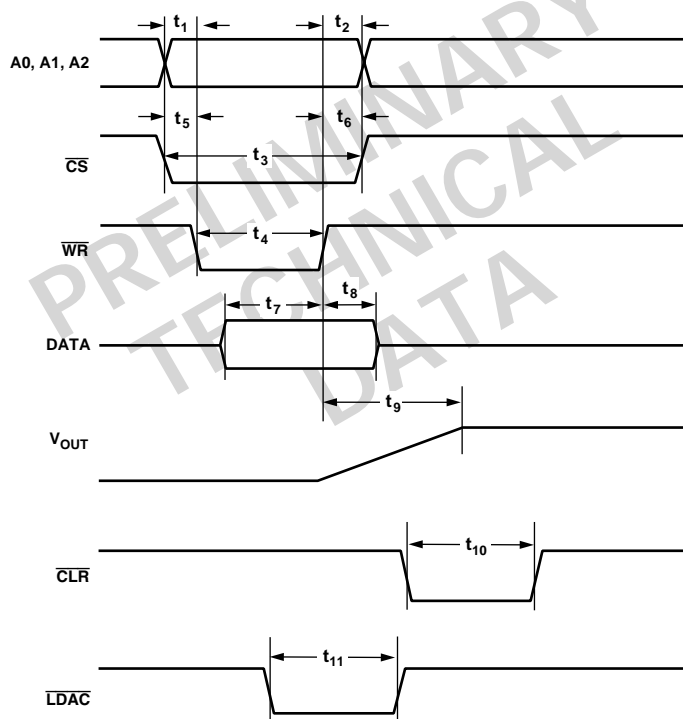


Figure 1. Timing Diagram

# AD7838

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to GND	-0.3 V to +6 V
V <sub>SS</sub> to GND	+0.3 V to -6 V
Digital Inputs to GND	-0.3 V to V <sub>DD</sub> +0.3 V
REF <sub>xx</sub>	DUTGND - 0.3 to V <sub>DD</sub> +0.3
DUTGND <sub>xx</sub>	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> +0.3
V <sub>OUT</sub>	V <sub>DD</sub> to V <sub>SS</sub>
Max Current Into REF <sub>xx</sub> Pin	±10 mA
Max Current Into Any Other Signal Pin	±50 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C

Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
PLCC Package, Power Dissipation	TBD mW
θ <sub>JA</sub> Thermal Impedance	48°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

### NOTES

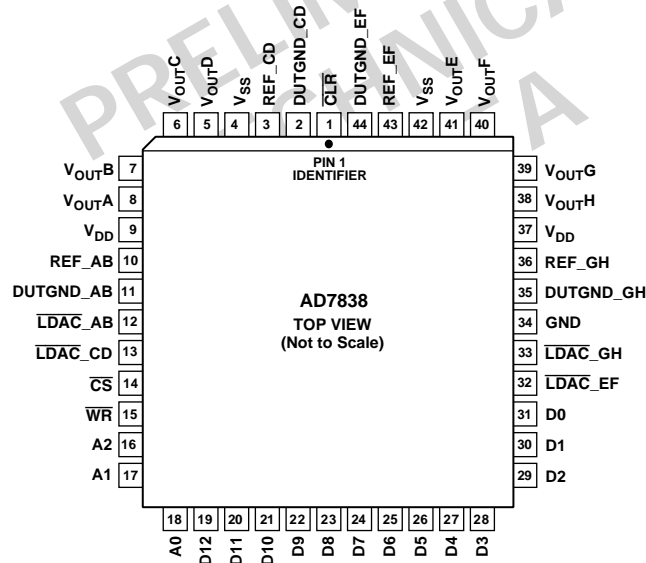
<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Transient currents of up to 100 mA will not cause SCR latchup.

## ORDERING GUIDE

Model	Temperature Range	Relative Accuracy (LSBs)	DNL (LSBs)	Package Description	Package Option
AD7838BP	-40°C to +85°C	±2	±1	Plastic Leaded Chip Carrier (PLCC)	P-44A

## PIN CONFIGURATION



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7838 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

